Design of a High-Swing, Low-Mismatch Charge Pump Using Super-Transistor Technique

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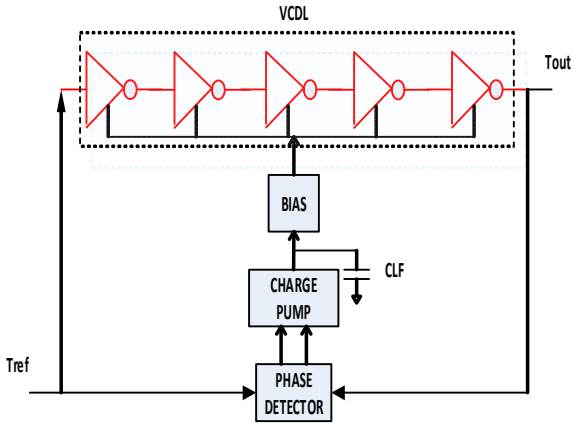
Abstract: - The charge pump (CP) circuit is a key element in a Fractional delay locked loop for high frequency synthesizer. Its function is to transform the Up and Down signals from the phase/frequency detector into current. In CMOS CPs, which have Up and Down switches made of p-channel MOS and n-channel MOS, respectively, the major back hit with CMOS charge pump is a current mismatch occurs when dumping the charge to the loop filter. This current mismatch of the CP in the FDLL generates fluctuations in the delay line, and in thus a large phase noise on the DLL output signals. In this paper a charge pump with good current mismatch by using super-transistor with high gain & high large output resistance is used as common source stage in complementary way to enhance the voltage swing at the output is presented and simulated in using 15 nm of technology by using gain boost feedback which help to achieve less than 1 % of current mismatches and large voltage swing proposed in this paper.

Index Terms: Gain-boosting charge pump (CP), Fractional delay locked loop (FDLL), phase frequency detector (PFD), loop filter (LF)

I. INTRODUCTION - Frequency synthesizers are a critical subsystem in modern RF Integrated Circuits (RFICs), enabling key functions such as clock generation, local oscillation, demodulation, and clock/data recovery. With the rapid growth of the Internet of Things (IoT), stringent power constraints in battery-operated and energy-harvested platforms have heightened the need for ultra-low-power design methodologies . Conventional frequency synthesizers, primarily implemented using Phase-Locked Loops (PLLs), typically dissipate power on the order of milliwatts. Such consumption significantly reduces battery life in portable systems, where the continuous operation of synchronous circuits is a major energy drain [2]. Moreover, PLL architectures require several passive analog components—such as resistors and capacitors—for loop stability and phase-noise suppression, leading to increased silicon area and additional power overhead. PLLs usually employ one of two main types of Voltage-Controlled Oscillators (VCOs): LC-tank oscillators and ring oscillators. LC-tank VCOs use a resonant circuit consisting of an inductor-capacitor (LC) network, along with a negative-resistance active device to compensate for inherent losses in each oscillation cycle, thereby satisfying the Barkhausen criterion. These oscillators are well known for their excellent phase-noise performance, making them suitable for high-precision applications. However, integrating high-quality inductors requires significant silicon area, making LC-based VCOs costly in terms of die size and less attractive for highly integrated systems. In contrast, ring-based VCOs provide a compact and scalable alternative, well-suited for dense System-on-Chip (SoC) integration. They offer lower power consumption and reduced area overhead compared to LC-based designs but suffer from higher susceptibility to phase noise and increased sensitivity to process, voltage, and temperature (PVT) variations. These limitations arise from their reliance on delay stages and parasitic effects, which can degrade frequency stability. The Delay-Locked Loop (DLL), first introduced in the early 1960s, was originally used for precise clock and data alignment in large-scale integrated circuits (ICs). Beyond timing synchronization, DLLs are also employed to generate multiphase clock signals essential for various timing-critical digital systems. By incorporating edge-combiner circuits or auxiliary digital logic, a DLL can be adapted to function as a frequency synthesizer, producing output frequencies that are integer multiples of the reference frequency. Compared to PLL-based designs, DLL-based frequency synthesizers offer advantages in design simplicity and reduced reliance on analog components, thanks to their inherently digital-centric architecture [1]-[5]. However, DLLs lack the architectural flexibility of PLLs with programmable frequency dividers and often require a large number of logic gates to achieve desired frequencies, especially at higher resolutions.

This brief presents an alternative to conventional PLL-based frequency synthesizers by employing a modified Delay-Locked Loop (DLL) architecture. The proposed design leverages the low power consumption and compact footprint of ring-oscillator-based Voltage-Controlled Oscillators (VCOs), while maintaining first-order control loop dynamics. This is achieved through a digital circuit that emulates a conventional Voltage-Controlled Delay Line (VCDL) within the feedback path. The oscillation frequency is precisely tuned using a simple biasing circuit, which adjusts the equivalent delay line to ensure both frequency stability and accurate output control.

A DLL is fundamentally a feedback system that synchronizes the delay of an output signal relative to a reference, aligning their phases without requiring a conventional oscillator. In applications demanding precise delay synchronization between periodic signals, DLLs are often preferred over Phase-Locked Loops (PLLs) due to their inherent simplicity. As a first-order system, the DLL is unconditionally stable, offering advantages in design robustness and reduced implementation complexity [6]. Furthermore, DLLs generally exhibit lower supply sensitivity and reduced phase noise compared to PLLs, making them particularly attractive for precision timing applications where noise minimization is critical [7].



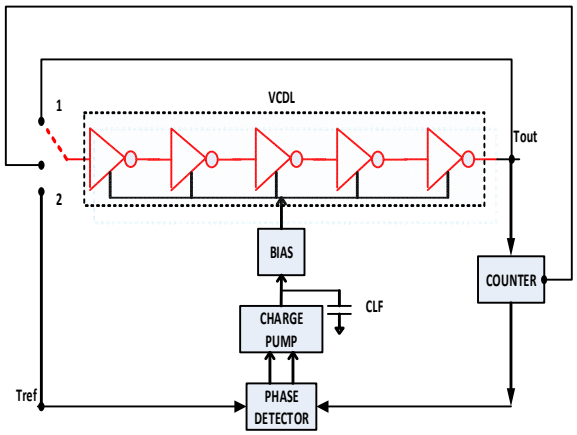


Fig 1. Standard delay -locked loop circuit block diagram **Fig 2. Fractional DLL block diagram**

In a conventional DLL, Figure 1 the output frequency is constrained to be equal to or less than the reference frequency, as the delay line is inherently passive. To enable synthesis of output frequencies higher than the reference, architectural modifications are required. In the proposed design, the VCDL is replaced with a current-starved inverter chain that can operate in two distinct modes: as a tunable delay element (DLL mode) or as a ring oscillator (frequency synthesis mode). A digital decision logic dynamically selects the operational mode. This modified delay line architecture, first introduced in [8] and later refined in subsequent implementations [3], preserves the DLL's first-order stability while incorporating a state machine to configure the output frequency. This ensures phase alignment with the reference input, while enabling frequency generation beyond the reference clock. A conceptual block diagram of the Frequency-Locked DLL (F-DLL) is shown in Figure 2. Most of the building blocks in the proposed architecture remain identical to those of a conventional DLL. The additional digital logic integrated into the VCDL enables dual-mode functionality: operating as a ring oscillator in self-looped configuration or as a standard delay line when the feedback path is open. This reconfigurability significantly enhances circuit versatility, providing greater flexibility than traditional PLL-based frequency synthesizers. Consequently, the architecture is well suited for wideband frequency synthesis applications that demand fine resolution and dynamic scalability [6],[8]. The proposed F-DLL consists of several key components: a Phase/Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF), and a Ring Oscillator. The oscillator output is fed back to the PFD, where it is compared against the reference signal. The PFD generates two digital control pulses—Up and Down—whose widths are proportional to the phase and frequency difference between the reference and the oscillator output.

The charge pump (CP) converts the digital pulses from the phase/frequency detector into differential current signals, which are then integrated by the loop filter (LF) to produce a control voltage. This voltage is applied to the ring oscillator, tuning its oscillation frequency accordingly. However, mismatches between the sourcing and sinking currents of the CP—caused by variations in the drain–source voltages of p-channel and n-channel MOSFETs—can result in net charge imbalances. These imbalances lead to fluctuations in the LF output voltage, particularly during phase acquisition and lock-in. Such current mismatches introduce spurious tones and increase phase noise in the ring oscillator output, thereby degrading the spectral purity of the synthesized signal [9]. The problem becomes more pronounced under non-ideal switching conditions or when the loop filter bandwidth is narrow.

Several CP architectures have been proposed to address these limitations:

- **Basic charge pump** – A simple topology with minimal circuitry but prone to current mismatch.
- **Current-mirror-based charge pump** – Uses current mirrors to improve the balance between sourcing and sinking currents.
- **Cascode charge pump** – Adds cascode transistors to increase output impedance and reduce mismatch.
- **Gain-boosted charge pump** – Employs operational amplifiers or gain stages to enhance node gain and improve current matching.
- **Switched-capacitor charge pump** – Replaces current sources with capacitors and switches for improved low-voltage operation.
- **Regulated cascode charge pump** – Combines cascode devices with feedback regulation (e.g., op-amp-based) for precise control.

Traditional CP designs often employ cascade [10],[11],[12] or low-voltage cascode topologies [13] to improve output impedance, thereby mitigating current mismatch. These techniques typically achieve matching accuracy within ~2% of the sourcing/sinking current differential. Higher performance can be obtained using operational amplifier–assisted CPs, which reduce mismatch to below 1%; however, these implementations incur additional complexity, occupy larger silicon area, and may introduce instability due to amplifier oscillations [10], [11].

Alternative approaches include differential CPs combined with active loop filters and common-mode feedback, which further enhance matching performance [12]. Nevertheless, these require additional analog circuitry—such as operational amplifiers, precision reference generators, and summation circuits—resulting in higher system complexity and power consumption. Another method involves incorporating a replica charge pump with a bias generator to actively compensate for mismatch down to 1% [12]. While effective, this approach increases design overhead and extends lock acquisition time. Similarly, designs employing a secondary CP with a modified PFD can correct mismatch [13] – [16], but are susceptible to process-induced mismatches between the primary and compensation CPs, which may reintroduce current imbalance and compromise overall performance.

II.GAIN-BOOSTING CP

Traditional CMOS charge pumps (CPs) typically use PMOS and NMOS transistors as the Up and Down switches, respectively. However, this setup often leads to current mismatches due to the drain–source voltage differences between the PMOS and NMOS transistors when discharging into the loop filter (LF). There are three configurations of CMOS based charge pump - Drain switched charge pump, Source switched charge pump and Gate switched charge pump as shown in Figure 3. each configuration has its own advantages and disadvantages as described in table 1.

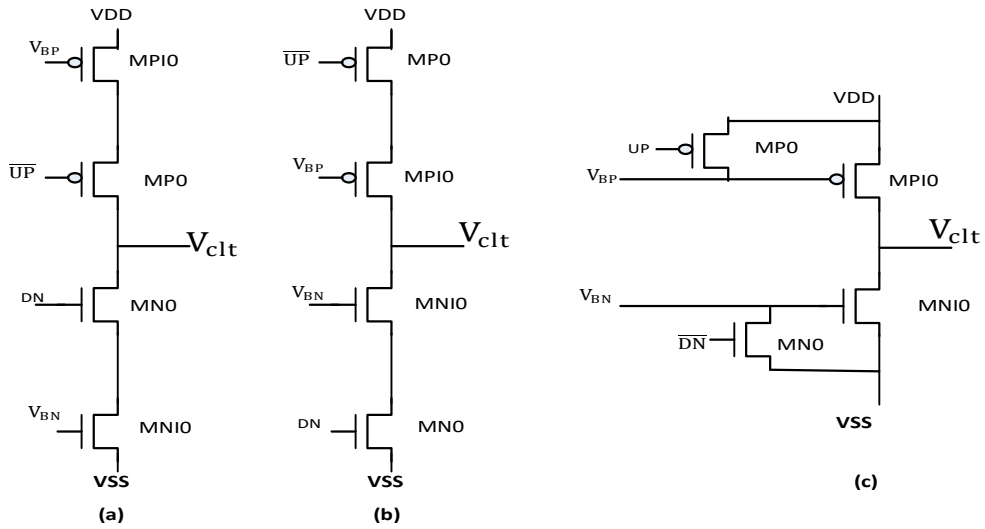


Figure 3 (a) Drain switched charged pump (b) Source switched charge pump (c) Source switched charge pump

Source Switched Charge Pump --	Drain Switched Charge Pump --	Gate Switched Charge Pump

Fastest transition charge pump as Switched CMOS toggle between linear to saturation, but limited Vclt swing due to small W/L ratio of switch MOSFET as increasing W/L of switch MOSFET leads to unequal rise and fall time at Vclt, and other disadvantage with large W/L it will increase overall parasitic capacitance at o/p load this will increase overall capacitance at o/p loop filter and clock feed through, and leads to delay in response. So, there must be tradeoff between W/L ratio.	Larger transition time as compared to source switched charge pump as switch CMOS toggle between cutoff to saturation. The advantage with drain switch is max swing Vclt and minimum clocked feedthrough as the W/L of current source is small, but the W/L ratio of Switch CMOS is large which leads to large power dissipation as compared to counterpart charge pump.	-- Gate switched charge pump have the largest Vclt swing, speed of transition is limited due to current source CMOS has to switch from cutoff to saturation, it has minimum clockfeed through due to minimum internal capacitance offered. Here to enhance the transition time we have to use large W/L ratio for current source CMOS. But it increases the clockfeed through.

In the above figure MPIO/MNIO work as current source MOSFET and MPO/MNO work as switch MOSFET. The source-switched approach is commonly used in high-precision charge pumps designed for low-phase noise and low-spurious phase-locked loops (PLLs) [17],[18]. In addition to addressing the concerns previously mentioned, this architecture offers several advantages, including faster switching speeds and reduced dependency on output voltage. These improvements lead to enhanced linearity, lower charge injection, and overall better PLL performance.

Analysis of Source switched charge pump Fig4 (a) shows the basic diagram of source switched charge pump, when UP=H, DN =L $I_{UP} = I_{CP}$, UP=L, DN =H $I_{DN} = -I_{CP}$ in other case $I_{CP} = 0$. Fig4 (b) current source is replaced by voltage controlled current source MOSFET, with control voltage V_{BP}, V_{BN} , Now to generate this stable voltage for constant current source we need biasing circuit which shown in fig4 (c) this will generate required bias voltage which force to generate desired I_{CP}, for the analysis of the source switch ed charge pump lets take the source node of current source MOSFET as V_y and V_x .

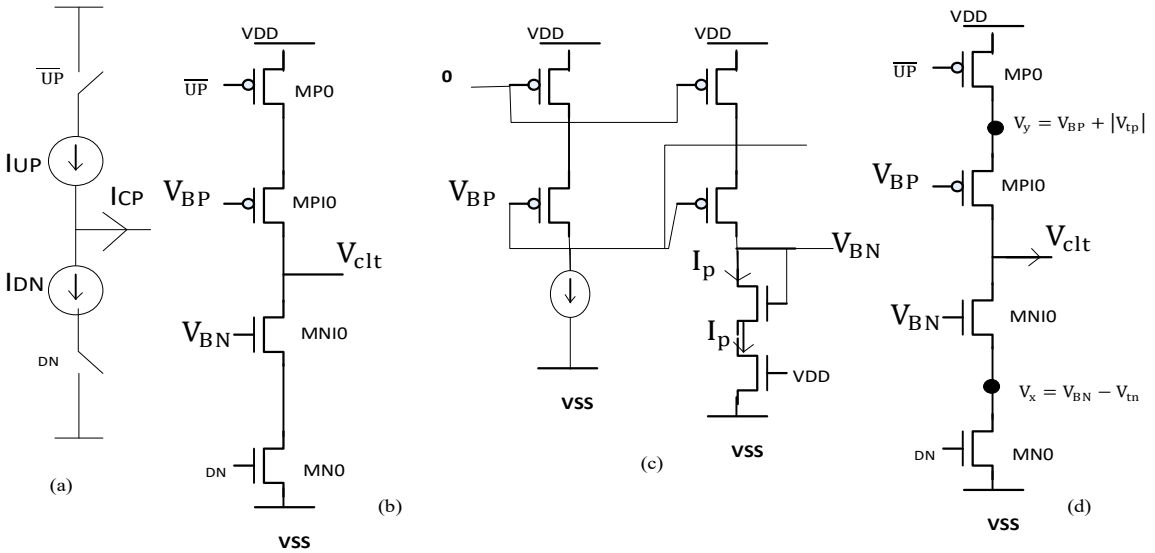


Figure 4. (a) basic diagram of source switched CP (b)Voltage controlled Source switched CP (c)biased voltage circuit with voltage controlled Source switched CP (d) Node analysis diagram voltage controlled Source switched CP

$$V_y = V_{BP} + |V_{tp}| \text{ and } V_x = V_{BN} - V_{tn}$$

During the off state (UP=L, DN =L and UP=H, DN =H) let V_{SD} /V_{DS} of PMOS/NMOS current source must be large so that it quickly switches to saturation region from linear region to achieve this W/L ratio is large. Let if

current source MOS have larger W/L ration and switch MOSFET have smaller W/L ratio during normal operation, this limits the V_{clt} swing, and we want large V_{clt} swing for which V_{SD} /V_{DS} current source must small which leads to smaller W/L ratio, so there must be trade-off between transition speed and output voltage swing.

$$V_{SD} \geq V_{GS} - |V_{tp}|$$

$$V_y - V_{clt} \geq V_y - V_{Bp} - |V_{tp}|$$

$$V_{clt} \leq V_{Bp} - |V_{tp}| \quad \text{----- (1)}$$

And for normal operation $V_y - V_{Bp} - |V_{tp}| \geq 0$

$$V_y - |V_{tp}| \geq V_{Bp} \quad \text{----(2)}$$

From Equation 1 and 2 it implies that V_y controls V_{clt} .

For high V_{clt} swing V_y must be large and V_x must be small to achieve this W/L must be large. If switch size is large $V_y \sim vdd \; and \; V_x \sim 0$ the problem associated with large W/L ratio is C_{gs} is large and this large capacitance is hard to drive by PFD(Phase Frequency Detector In DLL) to drive this large value buffer must be inserted in between PFD and charge pump it will increase the power consumption as well as transition time of Switch MOSFET will increase and may leads to unequal rise and fall time. This large W/L of switching MOSFET will increase parasitic capacitance so extra load capacitance at output V_{clt} node will be added this will increase loop filter capacitance which increases the spur at output node. To decrease the spur we have to decrease the W/L ration of switch Mosfet.

In this brief, we introduce a novel CP design that incorporates a gain-boosting circuit, instead of using NMOS CS stage we integrate PMOS CS stage to increase the output swing as using PMOS CS stage decreases V_x and increase V_y of charge pump. Figures 5(a) shows basic diagram of gain boost circuit. Figure 5 (b) shows simplified equivalent circuit.

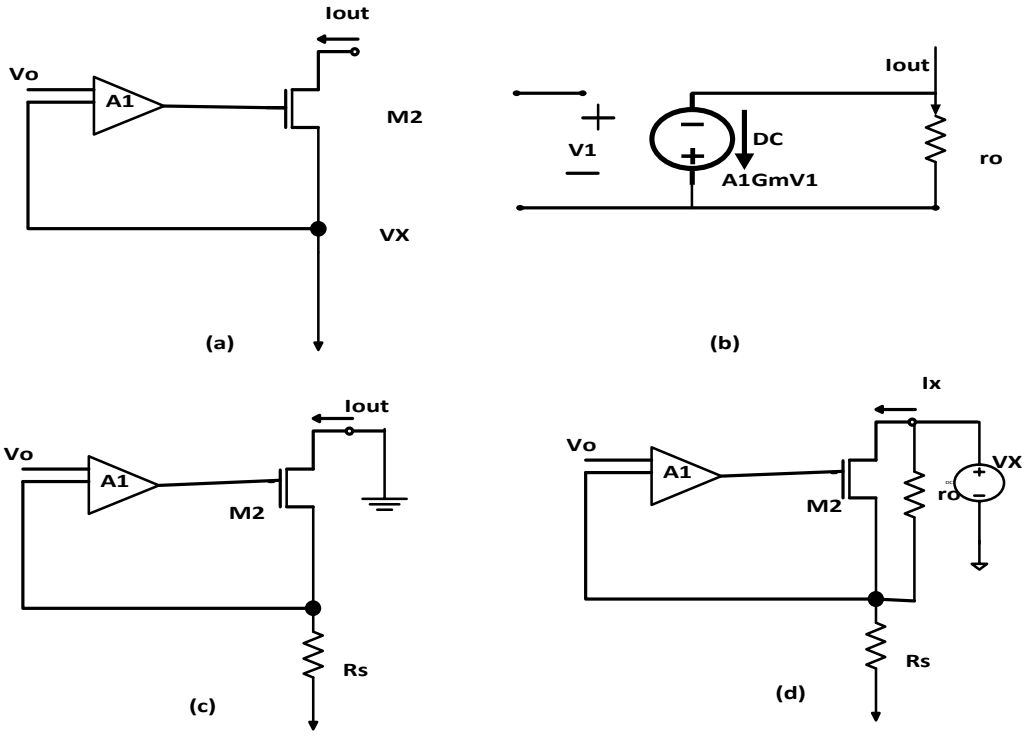


Figure 5. (a) Concept of the gain-boosting circuit. (b) small signal equivalent diagram (c) circuit to calculate transconductance (d) circuit to calculate output resistance

For Normal N-Mosfet voltage gain is given as,

$A_V = -g_m r_0$ but as due to amplifier as shown in fig 5 (a) the gate voltage is amplified by A, so the voltage gain

$A_V = -A1\, g_m r_0$ and we called it as super-transistor [19],[20], fig 5(b) shows the small signal model for super-transistor, fig 5(c) and fig 5(d) are used to calculate the transconductance and output resistance to verify the voltage gain.

Since R_s carries I_{out}, so the gate voltage is given by $A1(V_{in} - R_s I_{out})$ leads to $V_{gs} = A1(V_{in} - R_s I_{out}) - R_s I_{out}$

Hence, $I_{out} = g_m[A1(V_{in} - R_s I_{out}) - R_s I_{out}]$,

$$\frac{I_{out}}{V_{in}} = \frac{-g_m A1}{1 + (A1 + 1)\, g_m R_s} \cong g'_m$$

As from fig 5(d) $I_x = I_x g_m(-A_1 R_s - R_s) - \frac{V_X - I_x R_s}{r_0}$,

$$R_0 = r_0 + (A1 + 1)\, g_m R_s r_0 + R_s \approx r_0 + (A1 + 1)\, g_m R_s r_0$$

So, for this super transistor, $A_V = -g'_m R_0 = \frac{-g_m A1}{1+(A1+1)\, g_m R_s} \times [r_0 + (A1 + 1)\, g_m R_s r_0] = -A1\, g_m r_0$

Figure 6(a) shows simplified gain boost circuit, super transistor is used as degenerative resistor, from above the output impedance equal to,

$$R_0 = r_{02} + (A1 + 1)\, g_{m2} r_{02} r_{01} + r_{01}$$

The short -circuit transconductance approx. equal to g_{m1} because resistance seems looking into source of M2,

So, gain $A_V \approx g_{m1}[r_0 + (A1 + 1)\, g_{m2} r_{02} r_{01} + r_{01}] \approx g_{m1}(A1 + 1)\, g_{m2} r_{02} r_{01}$

Circuit implementation of gain booting technique for a common source stage is shown in figure 6(b) and 6(c) using NMOS and PMOS as amplifier. If I_2 is ideal than gain of M_3

$|A_1| = g_{m3} r_{03}$ using above equation,

the gain $\left|V_{out}/V_{in}\right| \approx g_{m1}(g_{m3} r_{03} + 1)\, g_{m2} r_{02} r_{01}$

the potential at V_X is dictated by V_{gs2} rater than override of M1, this limit the V_X min voltage which must be greater than $V_{gs2} + (V_{gs1} - V_{th1})$ which is not good for output swing to overcome this limitation we considered PMOSCS stage for A_1, the gain boosting process is same and now $V_x = (V_{gs1} - V_{th1})$, this will improve the output swing of our charge pump [19], [20]. The proposed charge pump using PMOS CS stage is used for pulldown and NMOS CS stage is used for pullup in source switch charge pump. As shown in figure 7.

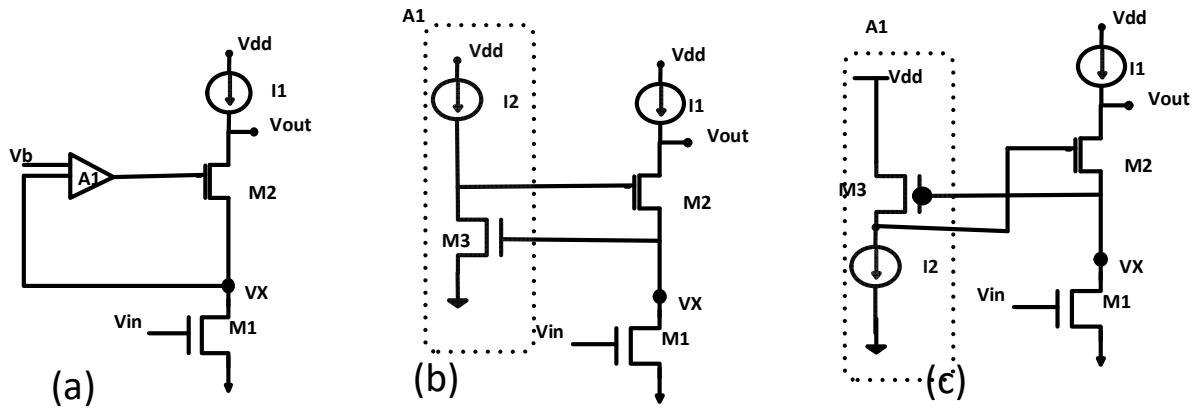


Figure 6. (a) Simplified gain-boosting circuit. (b) NMOS CS stage (c) PMOS CS stage

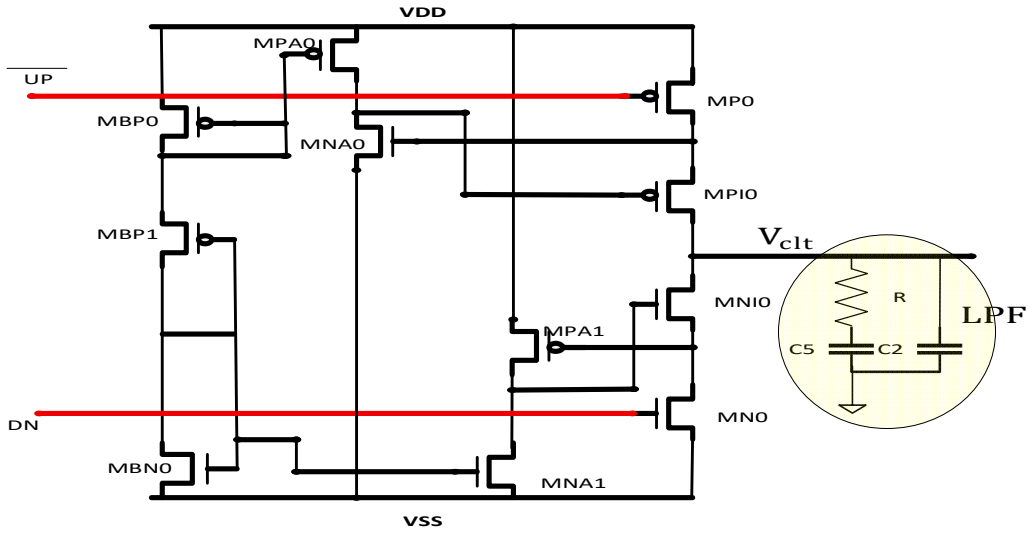


Figure 7. Proposed charge pump circuit

W/L ratio of FinFet in proposed design (W/N× no.Fins)				
MBP0=(288n/20n) × 3	MBP1=(288n/20n) × 3	MPA1 =(288n/20n) × 6	MPA0 =(288n/20n) × 8	MP0=(288n/20n) × 20
MBP00=(288n/20n) × 3	MBN0 =(288n/20n) × 1	MNA1 =(168n/20n) × 4	MNA0 =(168n/20n) × 4	MN00=(288n/20n) × 10
MN0 =(168n/20n) × 20	MP00 =(168n/20n) × 40	MPI0 =(288n/20n) × 7	MNI0 =(288n/20n) × 7	

The proposed CP is comparable to that of a triple-cascode structure. By incorporating this gain-boosting technique, a new charge pump (CP) can be designed with reduced sensitivity to channel length modulation. In the proposed CP, depicted in Fig 7 MPA0 and MNA1 function as current sources, MPA1 and MNA0 are employed as gain boost amplifier, When the DN signal is activated, MNA1 and MPA1 work together to realize PMOS CS the gain-boosting operation similarly MPA0 & MNA0. Work as NMOS CS gain boot amplifier. This configuration increases the overall output resistance of the CP circuit, thereby improving current matching performance and a using this boost amplifier in opposite fashion as compared to previous work [21], increase the voltage swing at the output. W/L ratio of the transistor are shown in table 2. One notable advantage of this gain-boosting approach is its compatibility with low supply voltages, as it does not require stacking additional cascode devices to enhance output resistance. However, due to the inherent differences in transconductance and output resistance between NMOS and PMOS transistors, the resistance enhancement achieved for each type may not be identical. This imbalance can result in current mismatch. To address this, both the DN and UP paths should be carefully designed to match each other, by properly selecting and tuning the values of the individual components.

III. Simulation Result-The proposed CP with gain boosting circuit is simulated by HSPICE using 15nm technology with 1V. Fig. 8 (a) shows the variation of the Up/Down current as the CP output voltage sweeps from 0 to 1V, respectively. These CPs show the current matching characteristics around .75-1 % of the sourcing/sinking current difference. Table 1. shows current mismatch leakage current charge injection, output impedance and total power consumption. Fig.6 shows the simulation result of the current matching around .45V ± .15V , did Montecarlo simulation with Vt as parametric variable and achieve around variation between 0.75-1 %

Table 2. shows the

Current mismatch (Vt variation 10%)	Leakage current	Charge injection and clock feedthrough	Output impedance	Power consumption
0.75-1 %	1m Amp	200ff	50k ohm	.5mW

simulation numeric values for different simulated parameter result

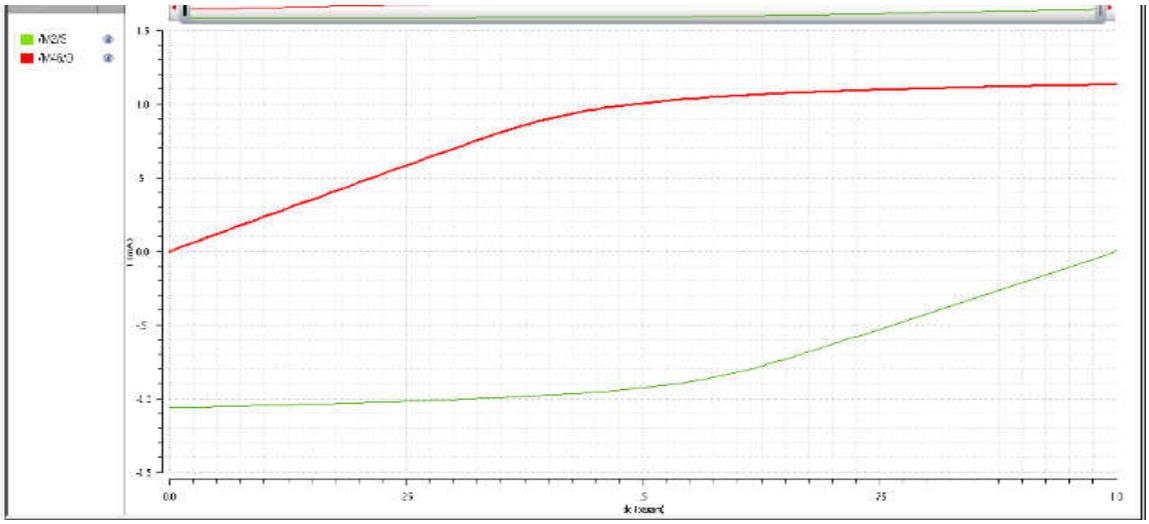


Figure 8. (a) output current at the O/P of CP used to calculate current mismatch.

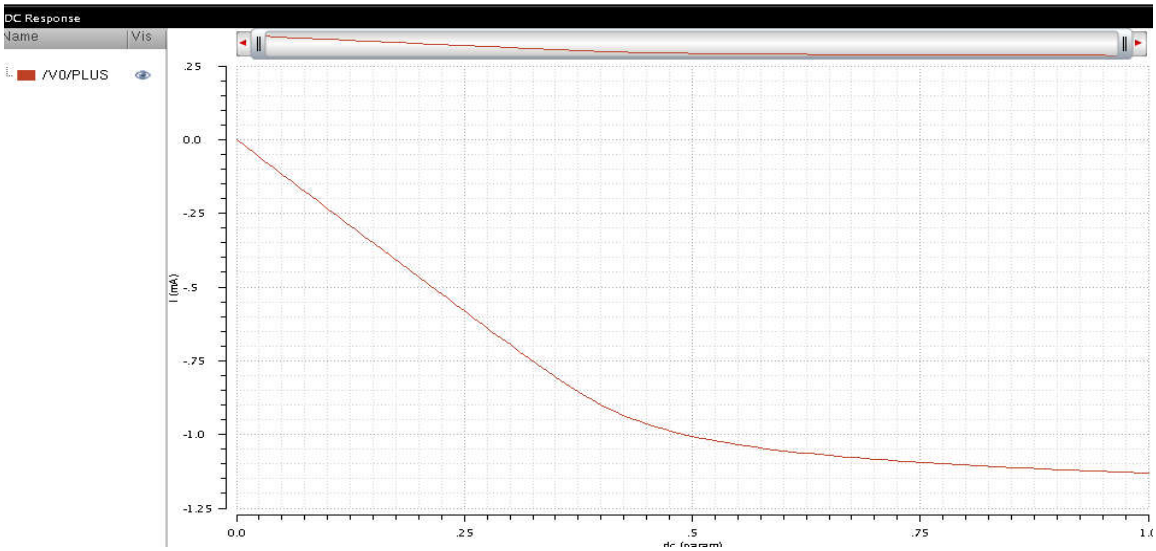


Figure 8. (b) output current variation which is used to find output impedance

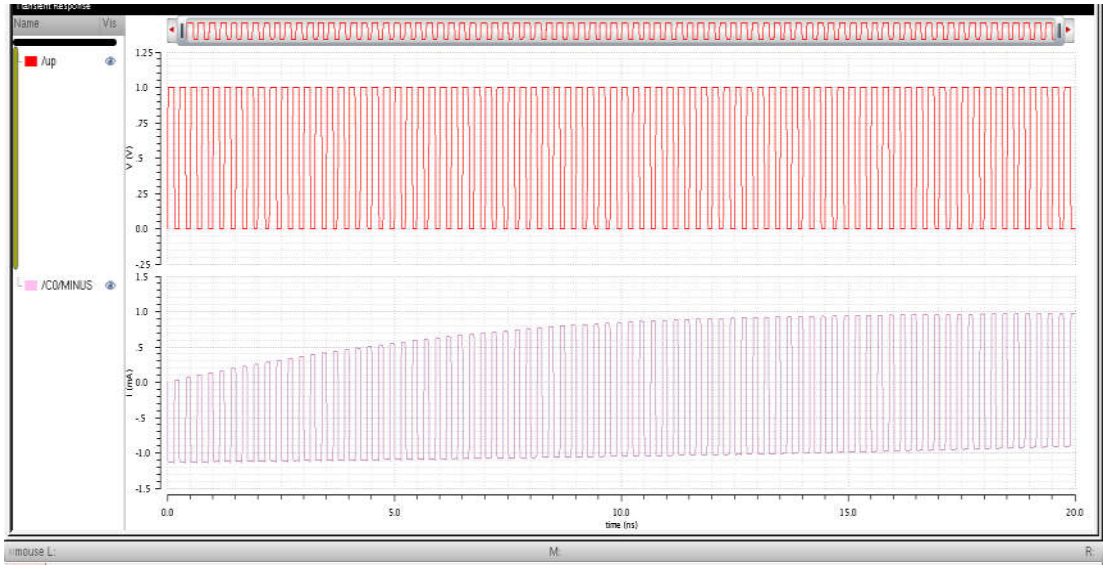


Figure 8. (c) Input/output wave diagram

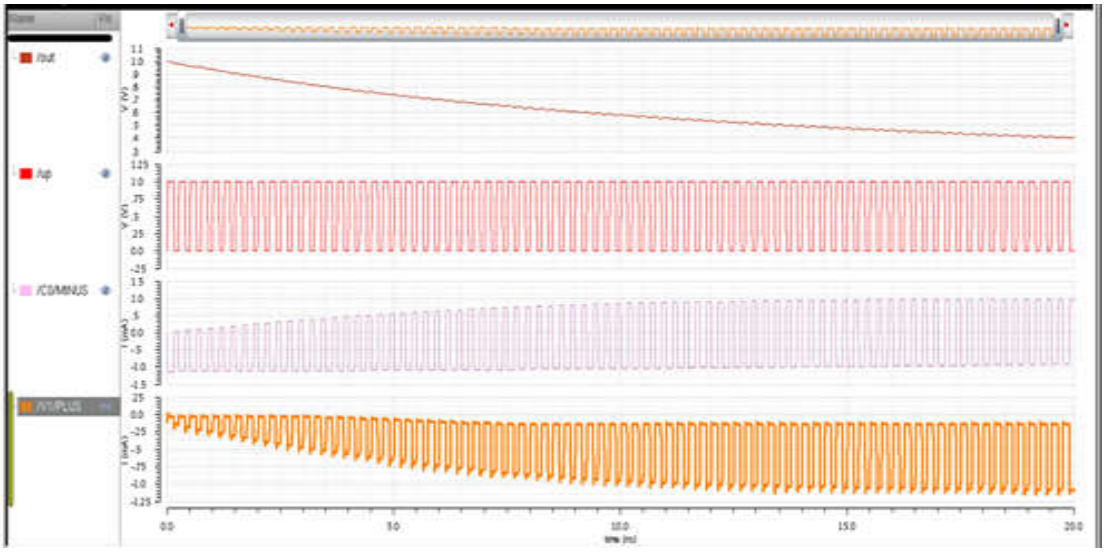


Figure 8 (d) the last wave diagram is the variation of current at supply voltage to calculate overall power consumption.

IV. Conclusion - Proposed CP achieves high output resistance through a simple gain-boosting circuit, eliminating the need for additional cascode stacking, operational amplifiers, feedback circuits, complex replica CPs, or extra compensation CPs. The maximum current difference between the Up and Down currents across the CP output voltage range of 0.8–1 V in a 15 nm process is less than 1%. The design maintains a current mismatch below 1% even under variations in process parameters, such as threshold voltage (Vt) shifts and temperature changes, including Vt increases due to transistor aging. This performance surpasses that of other CP architectures, which typically achieve around 1% current mismatch at best. Additionally, the proposed CP is well-suited for low supply voltage applications, as it avoids the complexity of cascode stacking.

V. REFRENCES:

1. J. Han, “A current-configurable charge pump with current mismatch reduction” Microelectronics Journal / Elsevier (article listing), 2024. sciencedirect.com
2. M. Guo, L. Wang, S. Wang, J. Lu and M. Cui, “A Low Mismatch Current Charge Pump Applied to Phase-Locked Loops,” Micromachines, vol. 15, no. 7, p. 913, 2024. mdpi.com

3. Adel Rezaeian1 · Gholamreza Ardeshir1 · Mohammad Gholami2 “A Low-Power and High-Frequency Phase Frequency Detector for a 3.33-GHz Delay Locked Loop” Circuits, Systems, and Signal Processing, 2019 pp 1-16.
4. M. Guo, L. Wang, S. Wang, J. Lu and M. Cui, “A Low Mismatch Current Charge Pump Applied to Phase-Locked Loops,” *Micromachines*, vol. 15, no. 7, p. 913, 2024.
5. P. B. Mane and S. N. Pawar, “An Ultra Low Current Mismatch Charge Pump and Loop Filter in 0.18 µm CMOS Process for Low Spur PLL Applications,” International Journal of Engineering Trends and Technology (IJETT), vol. 69, no. 6, 2021. ijettjournal.org.
6. H. Jayakumar, K. Lee, W. S. Lee, A. Raha, Y. Kim, and V. Raghunathan, “Powering the Internet of Things,” in Proc. Int. Symp. Low Power Electron. Design, 2014, pp. 375–380.
7. M. Liu, R. Ma, S. Liu, Z. Ding, P. Zhang, and Z. Zhu, “A 5-GHz low-power low-noise integer-N digital subsampling PLL with SAR ADC PD,” IEEE Trans. Microw. Theory Techn., vol. 66, no. 9, pp. 4078–4087, Sep. 2018.
8. Y. Deval and F. Rivet, “A balanced logic routing block for factorial-DLL based frequency generation,” in Proc. 29th Symp. Integr. Circuits Syst. Design Chip Mountains, 2016, pp.1–4.
9. Jeffrey Prinzie, Stefan Biereigel, Szymon Kulis, Pedro Leitao, Paulo Moreira “ Source switched Charge-Pump PLLs for High-Dose Radiation Environments” IEEE Transactions on Nuclear Science, 2023, p-p 590 - 595
10. H. Arora, N. Klemmer, J. C. Morizio, and P. D. Wolf, “Enhanced phase noise modelling of fractional-N frequency synthesizers,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 2, pp. 379–395, Feb. 2005.
11. P. Larsson, “A 2–1600 MHz CMOS clock recovery PLL with lowVdd capability,” IEEE J. Solid-State Circuits, vol. 34, no. 12, pp. 1951–1960, Dec. 1999.
12. W. Rhee, B.-S. Song, and A. Ali, “A 1.1 GHz CMOS fractional-N frequency synthesizer a 3-bit third-order A modulator,” IEEE J. Solid-State Circuits, vol. 35, no. 10, pp. 1453–1460, Oct. 2000.
13. R. Ahola and K. Halonen, “A 1.76 GHz 22.6 mW A fractional-N frequency synthesizer,” IEEE J. Solid-State Circuits, vol. 38, no. 1, pp. 138–140, Jan. 2003.
14. I. A. Young, J. K. Greason, and K. L. Wong, “A PLL clock generator with 5 to 110 MHz of lock range microprocessors,” IEEE J. Solid-State Circuits, vol. 27, no. 11, pp. 1599–1607, Nov. 1992.
15. J.-S. Lee, M.-S. Keel, S.-I. Lim, and S. Kim, “Charge pump with perfect current matching characteristics in phase-locked loops,” Electron. Lett., vol. 36, no. 23, pp. 1907–1908, Nov. 2000.
16. N. Da Dalt and C. Sander, “A sub picosecond jitter PLL for clock generation on 0.12- um digital CMOS,” IEEE J. Solid-State Circuits, vol. 38, no. 7, pp. 1275–1278, Jul. 2003.
17. H. Huh, Y. Koo, K. Y. Lee, Y. Ok, S. Lee, D. Kwon, J. Lee, J. Park, K. Lee, D. K. Jeong, and W. Kim, “A CMOS dual-band fractional-N synthesizer with reference doubler and compensated charge pump,” in Proc. IEEE Int. Solid-State Circuit Conf., 2004, vol. 1, pp. 100–101.
18. S. Pamarti, L. Jansson, and I. Galton, “A wideband 2.4 GHz Delta–Sigma fractional-N PLL with 1-Mb/s in-loop modulation,” IEEE J. Solid-State Circuits, vol. 39, no. 1, pp. 49–62, Jan. 2004.
19. B. Razavi, “The Delay-Locked Loop — A Circuit for All Seasons,” IEEE Solid-State Circuits Magazine, Summer 2018.
20. B. Razavi, “Analog CMOS Integrated Circuits,” IMcGraw-Hill Education 2015.
21. Young-Shig Choi and Dae-Hyun Han “Gain-Boosting Charge Pump for Current Matching in Phase-Locked Loop IEEE Transactions On Circuits And Systems—Ii: Express Briefs, Vol. 53, No. 10, October 2006